A Brief History of Memories in Space from a SEE (Single Event Effects) Perspective

Gary Swift, JPL/CalTech

The use of large memory arrays in space requires cognizance of the problems caused by the radiation environment, particularly SEE or single event effects. Of course, the definition of "large" has grown rapidly as ICs have improved. Concurrently, the preferred types of devices changed along with the SEE problems and solutions, as can be illustrated by various JPL-designed spacecraft. Originally, the IC memories used in space applications were bipolar SRAMs. These were replaced by CMOS SRAMs for a while (Galileo main memory), but now the largest arrays consist of DRAMs (the Cassini solid-state recorder). Looking forward, one can anticipate that these will be supplanted (or supplemented) by flash devices, as, for example, is envisioned for the X2000 non-volatile memory slice. The main SEE problems have changed as well, starting with simple cell upset, moving to latchup, then functional interruptions, multiple cell upset, and stuck bits. Currently, the SEE challenges with flash memories involve the extra device complexity (the various results of upsetting the state machine) and new destructive effects apparently related to the on-chip high voltages needed for erasure and programming.

SEE rates in space are predicted by measuring device susceptibility in ground testing and folding those results together with the expected radiation environment. During testing, the device-under-test is bombarded with accelerated beams of known ions to determine the minimum ionization deposition (threshold linear energy transfer or LET_{th}) and to measure the event probability (in terms of susceptible area or cross section) for ions depositing above the minimum charge. In practice, this testing requires not only knowledge of the device and its intended system use but also details of the SEE mechanism.

Consider simple cell upset. The architectures of the memory element itself differ between the various device types and thus, the mechanism of cell upset (single event upset or SEU) differs, but the starting point is the same: the ionization trail from an ion strike injects a transient into the circuit which responds and settles back to quasi-steady state. When the final state is different from the initial, the cell has been "upset" and a zero changed to a one (or vice versa). Understanding the circuit response of the storage element gives insight into hardening against upset as in, for example, resistive-hardening of the SRAM cell. Another solution to cell SEUs is incorporation of increasingly sophisticated error correction capability. However, as cell density scales, a new problem of multiple bit upsets (MBUs) from single ion strikes is becoming more important and impacts system architecture and performance. Flight experience with the Cassini spacecraft DRAM arrays is instructive: uncorrectable errors are more frequent than expected due to a system-architecture flaw.

Destructive SEEs are particularly important to understand and avoid. Examples range from Galileo-era 2kB SRAM studies of single event latchup (and its relationship to the epitaxial thickness) to the present commercial flash memories (8MB and larger) for use on the X2000 missions where cell upset is not really a problem anymore, but complicated and sometimes destructive effects need careful characterization and directly impact avionics system design and use.

*Works described here were carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.